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DYKEMA GOSSETT PLLC
FRANKLIN SQUARE, THIRD FLOOR WEST
1300 I STREET, NW
WASHINGTON, DC 20005

| EXAMINER | |
|---|---|
| DOTY, HEATHER ANNE | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2813 | |

DATE MAILED: 08/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/516,886 | RASMUSSEN ET AL. | |
| | Examiner | Art Unit | |
| | Heather A. Doty | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/3/2004,2/2/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

Claim 1 is objected to because of the following informalities: In claim 1, line 6, "photomaking" should be changed to "photomasking." Appropriate correction is required.

Claim 3 is objected to because of the following informalities: Claim 3 recites the limitation "the front side silicon" in line 7. There is insufficient antecedent basis for this limitation in the claim. Also in claim 3, the word "are" in line 10 should be deleted.

Claim 4 is objected to because of the following informalities: Claim 4 recites the limitation "the front-side electric insulation and the KOH etch-resistant metallic layers" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claim 4 also recites the limitation "the silicon" in 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 5 is objected to because of the following informalities: Claim 5 recites the limitation "the front side electric insulation and the KOH etch-resistant metallic layers" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim 10 is objected to because of the following informalities: Claim 4 recites the limitation "the CMOS structure" in line 3. There is insufficient antecedent basis for this limitation in the claim. Additionally, either "a" or "the" should be inserted between "of" in line 3 and "semiconductor" in line 4. Appropriate correction is required.

Claims 2, 5, 6, and 7 are objected to because of the following informalities: Claims 2, 5, 6, and 7 contain the word "preferably," followed by a limitation. It is not

clear to the examiner if the limitations following the word "preferably" are intended as claimed limitations. Since "preferably" is a vague word and implies that the limitations are not mandatory, the examiner has not given patentable weight to the limitations written as preferable in claims 2, 5, 6, and 7.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is not clear whether the feed-through recited in lines 1 and 3 is the same as the vias recited in line 6, since a feed-through and a via are both through-holes. The claim will be treated as best understood by the examiner.

Claims 2-10 are rejected for depending from claim 1.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Linder (WO 96/13062, published May, 1996).

Regarding claim 1, Linder teaches a process for generating a feed-through in a semiconductor wafer (110 in Figs. 4A-4P; p. 8, line 32), which has electric circuitry

embedded in a front surface (pads 106 in Fig. 4A), whereby a hole for the feed-through is generated by the combined use of a front-side protection layer (protective oxide or nitride layer 112 in Fig. 4B; p. 8, line 37 – p. 9, line 12) and a wet KOH etch process etching the hole from a back side of the wafer (Fig. 4F), where a photomasking process is used to define the vias (p. 10, lines 3-31), followed by deposition of via material (190 in Fig. 4O).

Regarding claim 3, Linder teaches the process as claimed in claim 1, and further teaches that the etch process from the back side takes place in a number of steps:

- a KOH-resistant layer is deposited on the back side (122 in Fig. 4C),
- openings for the through-holes are defined in the KOH etch-resistant layer using a photomasking process in alignment with the circuitry embedded in the front side silicon (Figs. 4D-4E),
- the openings for the through-holes are etched in the KOH-resistant layer (Fig. 4E), and
- the through-holes in the silicon re etched in a KOH bath (p. 10, line 22 – p. 11, line 4).

Regarding claim 4, Linder teaches the process as claimed in claim 3, whereby the front-side protection layer covering the through-hole is etched from the back side through the formed holes in the substrate (Fig. 4G).

Regarding claim 10, Linder teaches a device produced according to claim 1, wherein terminals for gaining contact with a CMOS structure embedded in the surface of the semiconductor wafer (p. 4, lines 20-22 teach CMOS circuitry) are placed on both

the back and front sides of the wafer (terminal 58 is on the front side of the middle wafer in Fig. 2, terminal 56 is on the back side), and where a feed-through connects the terminals on the back side with the CMOS circuitry embedded in the front side of the wafer (feed-through 40 with conductor 46 connects the terminal 56 with the circuitry embedded on the top of the middle wafer in Fig. 4). The term "amplifier" has not been given patentable weight because this term appears only in the claim preamble, and no limitation in the body of the claim restricts the device to having structure specific to an amplifier. See MPEP 2111.02.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Linder (WO 96/13062, published May, 1996) in view of Munch (U.S. 6,538,328).

Regarding claim 2, Linder teaches the process as claimed in claim 1, and further teaches that the front-side protection layer comprises an electrical insulation layer (oxide or nitride), but does not teach that it also comprises a KOH-resistant metallic layer.

Munch teaches using a KOH-resistant metallic layer comprises a TiW layer and a Au layer (column 3, lines 25-42) to protect the front side of a wafer having contact pads during a back-side KOH etch.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the process taught by Linder, and further add a protective KOH-resistant metallic layer to the front side of the surface to protect the contact pads, and to avoid the use of additional mechanical equipment to protect the wafer, as expressly taught by Munch (column 2, lines 39-49).

Regarding claim 5, Linder teaches the process as claimed in claim 3 (note 35 U.S.C. 102(b) rejection above), but does not teach that the front-side protection layer covering the through-holes are etched from the front side.

Munch teaches forming a front-side protection layer of TiW and Au, etching a through-hole using KOH through the back side of the wafer, and then etching the front-side protection layer from the front (Fig. 3G, column 5, lines 35-42).

Therefore, at the time of the invention, it would have been obvious to use the process taught by Linder, and further etch the front-side protection layer from the front, as taught by Munch, since the method taught by Munch provides many advantages, such as reduction in manufacturing costs due to the ease of batch-production of devices (column 5, lines 27-30).

Regarding claim 6, Linder and Munch together teach the method of claim 5. Linder further teaches that the inside of the etched holes and back side of the wafer are covered with an insulation layer (PECVD-deposited insulation layer 170 in Fig. 4J; p. 11, lines 30-34), and the insulation layer is covered with a plating base (TiW and Au layer 172 in Fig. 4K; p. 11, lines 35-36).

Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Linder (WO 96/13062, published May, 1996) in view of Kahle, II, et al. (hereinafter "Kahle et al.", U.S. 5,733,479).

Regarding claim 8, Linder teaches the process as claimed in claim 1, whereby the photomasking process comprises deposition of a photoresist, whereby the deposited photoresist is exposed through a mask defining the negative image of the feed-through back and front side respectively, and where the photoresist is developed and the feed-through is subsequently formed by deposition of metal (Linder teaches using conventional photolithography—p. 12, lines 20-23; Fig. 4N—which involves depositing photoresist (shown in Fig. 4N), and exposing the deposited photoresist through a mask defining the negative image of the feed-through back and front sides (results in the photoresist pattern shown in Fig. 4N—although Linder does not expressly teach using either positive or negative photoresist, a mask used with either would define both the negative and positive images of the feed-through, since "defining" the image does not limit the mask to being either light-field or dark-field).

Linder does not teach that the photoresist is electrodeposited.

Kahle et al. teaches that it is advantageous to electrodeposit photoresist in a substrate having holes because the photoresist does not plug the holes (column 1, lines 38-42).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the process taught by Linder, and further use

electrodeposited photoresist to avoid plugging the through-hole, as taught by Kahle et al.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Linder (WO 96/13062, published May, 1996) in view of Kahle, II, et al. (hereinafter "Kahle et al.", U.S. 5,733,479) as applied to claim 8 above, and further in view of Gross (U.S. 6,458,696).

Regarding claim 9, Linder and Kahle et al. together teach the process as claimed in claim 8, but do not teach that the feed-through is formed by deposition of Cu and Ni.

Gross teaches forming a feed-through in a substrate by depositing Cu and Ni (column 9, line 40 – column 10, line 9).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the process taught by Linder and Kahle et al. together, and further deposit Cu and Ni in the through-hole to form the feed-through. The motivation for doing so at the time of the invention would have been that these materials are appropriate for plating, using the method shown by Gross to effectively coat the surface of through holes having small diameters (column 2, lines 53-58).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Linder (WO 96/13062, published May, 1996) in view of Munch (U.S. 6,538,328) as applied to claim 6 above, and further in view of Eldridge et al. (U.S. 2003/0045082).

Regarding claim 7, Linder and Munch together teach the method of claim 6. Linder further teaches taking care to prevent forming insulation material on the front

side originating from the PECVD process on the back side, but does not expressly teach removing whatever residual insulation material may form.

Eldridge et al. teaches sputter-cleaning a wafer to remove undesirable residual oxides (paragraph 0099).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the process taught by Linder and Munch together, and further use sputter-cleaning to remove residual insulator from the PECVD process, since Eldridge et al. teaches that it is known in the art of semiconductor processing to use sputter-etching to remove undesirable residual insulating materials from wafers.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

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CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800